CLAIMS

What is claimed is:

1. A method for fabricating a high voltage device, a low voltage device and a memory device of an integrated circuit, comprising:

forming a source region and a drain region associated with a gate region for each of a high-voltage (HV) device, a low-voltage (LV) device and a non-volatile memory (NVM) device, the HV, LV and NVM devices each electrically isolated by a field oxide region located adjacent the source and drain regions;

forming field implant regions under the field oxide regions;

forming a blanking layer on the field oxide regions and a portion of the source and drain regions associated with the HV and NVM devices;

depositing a metal layer on the gate regions, the blanking layer and exposed portions of the source and drain regions not covered by the blanking layer; and

forming metal salicide regions in the gate regions and the exposed portions of the source and drain regions.

2. The method of claim 1, further comprising the field implant regions located a predefined distance from an active edge of the source and drain regions associated with the HV and NVM devices.

3. The method of claim 1, further comprising the field implant regions associated with the HV and NVM devices including a width less than the field oxide regions.

4. The method of claim 1, further comprising the metal salicide regions associated with the HV and NVM devices located a predetermined distance from an active edge of the respective source and drain regions.

5. The method of claim 1, further comprising the metal layer selected from the group consisting of titanium, cobalt, tungsten, platinum, nickel and molybdenum.

6. The method of claim 1, wherein the blanking layer comprises an oxide.

7. The method of claim 1, wherein the blanking layer comprises a nitride.

8. The method of claim 1, wherein forming metal salicide regions comprises:

annealing the LV, HV and NVM devices to react the metal layer with the gate regions and the exposed source and drain regions; and

removing the metal layer on the field oxide regions.

9. The method of claim 1, further comprising:

implanting a dopant in the metal salicide regions; and

annealing the substrate to reduce resistivity of the metal salicide regions.

10. A method for fabricating a high-voltage device, a low-voltage device and a memory device of an integrated circuit, comprising:

forming a source region and a drain region associated with a gate region for each of a low-voltage (LV) device, a high-voltage (HV) device and a non-volatile memory (NVM) device, the LV, HV and NVM devices each electrically isolated by a field oxide region;

forming field implant regions under the field oxide regions, located a first predetermined distance from an active edge of the source and drain regions associated with the HV and NVM devices;

forming a blanking layer on the field oxide regions and a portion of the source and drain regions associated with the HV and NVM devices;

depositing a metal layer on the gate regions, the blanking layer and exposed portions of the source and drain regions; and

forming metal salicide regions in the gate regions and the exposed portions of the source and drain regions, the metal salicide regions located a second predetermined distance from the active edge of the source and drain regions associated with the HV and NVM devices.

11. The method of claim 10, further comprising the field implant regions associated with the HV and NVM devices including a width less than the field oxide regions.

12. The method of claim 10, further comprising the metal layer selected from the group consisting of titanium, cobalt, tungsten, platinum, nickel and molybdenum.

13. The method of claim 10, further comprising the metal layer including a thickness between approximately 100 angstroms and approximately 500 angstroms.

14. The method of claim 10, wherein the blanking layer comprises an oxide.

15. The method of claim 10, wherein the blanking layer comprises a nitride.

16. The method of claim 10, wherein forming metal salicide regions comprises:

annealing the LV, HV and NVM devices to react the metal layer with the gate regions and the exposed source and drain regions; and

removing the metal layer on the field oxide regions.

17. The method of claim 10, further comprising:

implanting a dopant in the metal salicide regions; and

annealing the LV, HV and NVM devices to reduce resistivity in the metal salicide regions.

18. An integrated circuit , comprising:

a source region and a drain region associated with a gate region for each of a low-voltage (LV) device, a high-voltage (HV) device and a non-volatile memory (NVM) device, the LV, HV and NVM devices each electrically isolated by a field oxide region located adjacent the source and drain regions;

a field implant region formed underneath each of the field oxide regions;

a blanking layer formed on the field oxide regions and a portion of the source and drain regions associated with the HV and NVM devices; and

a metal salicide region formed in each of the gate regions and exposed portions of the source and drain regions.

19. The integrated circuit of claim 18, further comprising the field implant regions located a predefined distance from an active edge of the source and drain regions associated with the HV and NVM devices.

20. The integrated circuit of claim 18, further comprising the field implant regions associated with the HV and NVM devices including a width less than the field oxide regions.

21. The integrated circuit of claim 18, further comprising the metal salicide regions located a predetermined distance from an active edge of the respective source and drain regions.

22. The integrated circuit of claim 18, further comprising the metal salicide regions selected from the group consisting of a cobalt salicide, a titanium salicide, a tungsten salicide, a platinum salicide, a nickel salicide and a molybdenum salicide.

23. The integrated circuit of claim 18, wherein the blanking layer comprises an oxide.

24. The integrated circuit of claim 18, wherein the blanking layer comprises a nitride.